What is claimed is:

1. A semiconductor integrated circuit having a logic circuit which comprises:

one or more first transistors for supplying electric charges to an external load via an output terminal; and

one or more second transistors for drawing electric charges from the load via the output terminal, and wherein:

in the logical operation of the logic circuit, the above supply and drawing of electric charges are executed according to combination of the states of a plurality of binary logic signals input from an external device; and

among all the transistors in the logic circuit, each transistor other than the first transistors for supplying electric charges has a threshold voltage value lower than that of each first transistor.

2. A semiconductor integrated circuit having an AND logic circuit which comprises:

a NAND circuit which includes:

parallel-connected first and second p-channel MOS FETs, where first and second input signals are respectively input into the gate electrodes of the FETs; and

a first n-channel MOS FET, where the first input signal is input into the gate electrode and an inverted signal of the second input signal is input into the source electrode, and

wherein the common drain electrode of the first and second p-channel MOS FETs and the drain electrode of the first n-channel MOS FET are

connected; and

an inverter circuit having a complementary MOS transistor structure for receiving an output signal from the NAND circuit and outputting an inverted signal of the received signal from an output terminal, where the complementary MOS transistor structure comprises a third p-channel MOS FET and a second n-channel MOS FET, and

wherein among all the MOS FETs in the AND logic circuit, each FET other than the third p-channel MOS FET has a threshold voltage value lower than the threshold voltage value of the third p-channel MOS FET.

3. A semiconductor integrated circuit having an AND logic circuit which comprises:

a NAND circuit which includes:

a first pMOS FET, where a fixed electric potential is applied to the gate electrode so as to keep the first MOS FET on; and

a first n-channel MOS FET, where a first input signal is input into the gate electrode and a second inverted input signal is input into the source electrode, and

wherein the drain electrode of the first p-channel MOS FET and the drain electrode of the first n-channel MOS FET are connected; and

an inverter circuit having a complementary MOS transistor structure for receiving an output signal from the NAND circuit and outputting an inverted signal of the received signal from an output terminal, where the complementary MOS transistor structure comprises a second p-channel MOS FET and a second n-channel MOS FET, and

wherein among all the MOS FETs in the AND logic circuit, each FET other

than the second p-channel MOS FET has a threshold voltage value lower than the threshold voltage value of the second p-channel MOS FET.

4. A semiconductor integrated circuit having a NOR logic circuit which comprises:

a first pMOS FET, where a first input signal is input into the gate electrode and an inverted signal of a second input signal is input into the source electrode; and

parallel-connected first and second nMOS FETs, where the first and second input signals are respectively input into the gate electrodes of the FETs, and wherein:

the drain electrode of first pMOS FET and the common drain electrode of the first and second nMOS FETs are connected; and

the threshold voltage value of each of the MOS FETs in the NOR logic circuit may be decreased.

5. A semiconductor integrated circuit as claimed in any one of claims 1 to 4, wherein the logic circuit is applied to a decoder circuit.

6. A semiconductor integrated circuit comprising:

a decoder area, positioned between adjacent memory cell areas, having one or more p-channel MOS FETs and one or more n-channel MOS FETs, wherein:

each of the p-channel MOS FETs and n-channel MOS FETs is arranged in a manner such that the direction of the gate width is perpendicular to the direction along which word lines extend in the memory cell areas.

7. A semiconductor integrated circuit as claimed in claim 6, wherein the p-channel

MOS FETs and the n-channel MOS FETs are aligned in a direction perpendicular to the direction along which word lines extend in the memory cell areas, in a manner such that the p-channel MOS FETs and the n-channel MOS FETs face each other.

8. A semiconductor integrated circuit comprising:

a decoder area, positioned between adjacent memory cell areas, having one or more p-channel MOS FETs and one or more n-channel MOS FETs, wherein:

the p-channel MOS FETs and the n-channel MOS FETs are aligned in a direction perpendicular to the direction along which word lines extend in the memory cell areas, in a manner such that the p-channel MOS FETs and the n-channel MOS FETs face each other.

9. A semiconductor integrated circuit as claimed in any one of claims 6 to 8, wherein the p-channel MOS FETs and the n-channel MOS FETs form a NAND circuit.

10. A semiconductor integrated circuit as claimed in any one of claims 6 to 8, wherein the p-channel MOS FETs and the n-channel MOS FETs form an AND logic circuit comprising a NAND circuit and an inverter circuit.

11. A semiconductor integrated circuit as claimed in any one of claims 6 to 8, wherein the p-channel MOS FETs and the n-channel MOS FETs form a NOR circuit.

12. A semiconductor integrated circuit as claimed in any one of claims 6 to 8, wherein a main power supply line for supplying electric power is provided in and along each boundary between the decoder area and each of the memory cell areas, and the

main power supply lines in the boundaries are connected via first sub power supply lines which cross the decoder area and extend parallel to the direction along which the word lines extend.

13. A semiconductor integrated circuit as claimed in claim 12, wherein:

the main power supply lines at both sides of a memory cell area are connected via second sub power supply lines which cross the memory cell area; and

the main power supply lines, and the first and second sub power supply lines form a wiring network for supplying electric power over the whole chip area of the semiconductor integrated circuit.

14. A semiconductor integrated circuit as claimed in any one of claims 6 to 8, wherein a main earth line for grounding is provided in and along each boundary between the decoder area and each of the memory cell areas, and the main earth lines in the boundaries are connected via first sub earth lines which cross the decoder area and extend parallel to the direction along which the word lines extend.

15. A semiconductor integrated circuit as claimed in claim 14, wherein:

the main earth lines at both sides of a memory cell area are connected via second sub earth lines which cross the memory cell area; and

the main earth lines, and the first and second sub earth lines form a wiring network for grounding over the whole chip area of the semiconductor integrated circuit.

16. A semiconductor integrated circuit as claimed in claim 12, wherein a main earth line for grounding is provided in and along each boundary between the decoder area and

each of the memory cell areas, and the main earth lines in the boundaries are connected via first sub earth lines which cross the decoder area and extend parallel to the direction along which the word lines extend.

17. A semiconductor integrated circuit as claimed in claim 16, wherein:

the main power supply lines at both sides of a memory cell area are connected via second sub power supply lines which cross the memory cell area;

the main power supply lines, and the first and second sub power supply lines form a wiring network for supplying electric power over the whole chip area of the semiconductor integrated circuit;

the main earth lines at both sides of a memory cell area are connected via second sub earth lines which cross the memory cell area; and

the main earth lines, and the first and second sub earth lines form a wiring network for grounding over the whole chip area of the semiconductor integrated circuit.